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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,284	08/05/2003	Brent Raymond Doyle	50191 (SE-1953-IP)	7084
7590	07/22/2004		EXAMINER	
CHARLES E. WANDS, ESQ. ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST, P.A. 255 SOUTH ORANGE AVENUE, SUITE 1401 P.O. BOX 3791 ORLANDO, FL 32802-3791			NGUYEN, MINH T	
			ART UNIT	PAPER NUMBER
			2816	
			DATE MAILED: 07/22/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

(P)

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/634,284	DOYLE, BRENT RAYMOND	

<b>Examiner</b>	<b>Art Unit</b>	
Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is **FINAL**.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 13-15 is/are allowed.
- 6) Claim(s) 1-5 and 7-11 is/are rejected.
- 7) Claim(s) 6 and 12 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

<ol style="list-style-type: none"> <li>1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</li> <li>2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.</li> </ol>	<ol style="list-style-type: none"> <li>4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.</li> <li>5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</li> <li>6)<input type="checkbox"/> Other: _____.</li> </ol>
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## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 9 and 13-14 are objected to because of the following informalities:

In claim 9, line 2, “energy” should be deleted so that the term be consistent with the term used on line 3 of claim 8.

In claim 13, line 12, “a capacitor” should be changed to -- an electrical energy storage device --, see line 13.

In claim 14, “a current source” should be changed to -- said current source --, see line 11 of claim 13.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,982,116, issued to Lee.

As per claim 7, Lee discloses a circuit (Fig. 2) for controllably asserting either internal clock signal (the output signal from the internal clock generator 34) or an external clock signal

(the output signal from the external clock signal 30) on a clock signal bus (the bus connected to the output of NAND gate 40) of an integrated circuit (column 2, lines 36-37) comprising:

an internal signal transport path (the path from the internal clock generator 34 to the clock signal bus) that is operative, the absence of the external clock signal being coupled to a prescribed conductor of said integrated circuit, to couple the internal clock signal as a default clock signal (column 3, lines 24-26, i.e., when the external clock is absent, node A is LOW, node B is HIGH, NAND gate 38 passes the internal clock signal) to the clock signal bus of said integrated circuit;

an external clock signal transport path (the path from the external clock generator 30 to the clock signal bus) that is operative, in response to the external clock signal being coupled to said prescribed conductor of said integrated circuit (column 2, line 62), to interrupt the coupling said internal clock signal (the existence of the external clock signal drives node A to HIGH, therefore, the internal clock path is blocked and the external clock path is enabled, column 3, lines 36-62 and column 4, lines 1-4) to said clock signal bus of said integrated circuit in and, in place thereof, to couple said external clock signal to said clock signal bus of said integrated circuit.

As per claim 8, the recited electrical storage device reads on capacitors C1 and C2 (Fig. 3), the recited discharge control circuit reads on switches 56, 58 and clock generator 62. The functional recitation on the last five lines is explicitly disclosed in column 3, lines 37-62).

As per claim 9, capacitor C1 stores energy provided by current source 50.

As per claim 10, see the operation description in column 3, lines 36-62, i.e., switches SW1 and SW2 are controlled by clock generator 62 to discharge the capacitors repeatedly (see waveform in Fig. 4) through GND.

As per claim 11, see equation disclosed in column 3, line 56. The recited predetermined reference voltage is the threshold voltage of inverter 52 (column 3, line 61).

As per claim 1, this claim is merely a method to operate the circuit having a structure recited in claim 1. Since Lee teaches the circuit, the method to operate is inherently disclosed.

As per claims 2-5, rejected for the same reasons noted in claims 2-11, respectively.

***Allowable Subject Matter***

3. Claims 6 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 is allowable because the prior art of record fails to disclose or suggest the inclusion of a discharge control circuit which generates a delayed version of the external clock signal and using a logical relationship between the external clock signal and the delayed version to control the discharge of the capacitor.

Claim 6 is allowable for the same reason noted in claim 12.

4. Claims 13-15 are allowed after claims 13-14 are amended to overcome the informality objections noted herein above. Claims 13-15 are allowed for the reasons noted in claim 12, i.e., inverting delay and logic circuit.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

 7/21/04

Minh Nguyen  
Primary Examiner  
Art Unit 2816